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(54) Improved positive charge pump

(57) A charge pump comprises a plurality of stages (S1-S4) connected in series, an input terminal (I) of the charge pump being connected to a voltage supply (VDD) and an output terminal (O) of the charge pump providing an output voltage higher than the voltage supply. Each stage comprises unidirectional current flow MOS transistor means (M1) connected between a stage input terminal (SI) and a stage output terminal (SO) allowing current to flow only from said stage input terminal to said stage output terminal, and a first capacitor (C1) with one plate connected to said stage output terminal and another plate driven by a respective first digital signal (B,D) periodically switching between ground and said voltage supply. The unidirectional current flow MOS transistor means (M1) of the stages have independent bulk electrodes (BUN), and a bias voltage generator circuit (2) is provided for biasing the bulk electrodes of said unidirectional current flow MOS transistor means at respective bulk potentials (B01,B2,B3) which become progressively higher going from the stages proximate to said input terminal to the stages proximate to said output terminal of the charge pump.

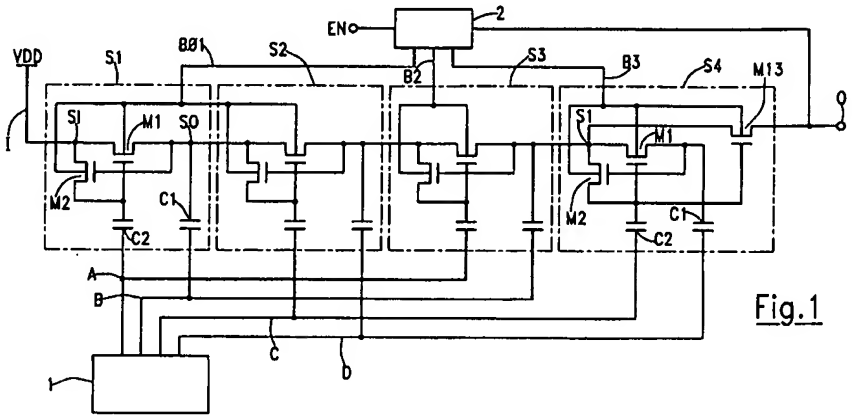

Fig.1

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Description

The present invention relates to an improved positive charge pump, particularly for the integration in CMOS integrated circuits such as non-volatile memory devices.

As known, a positive charge pump is a circuit suitable for generating, starting from a positive voltage having a predetermined value, a higher voltage.

Conventionally, a positive charge pump comprises a plurality of stages connected in series between an input terminal of the charge pump connected to a positive voltage supply and an output terminal of the charge pump. In the simplest case, each stage substantially comprises a diode-connected N-channel MOSFET and a capacitor having one plate connected to the source electrode of the MOSFET and another plate driven by a respective digital signal periodically varying between ground and the voltage supply.

In steady-state operation, the voltage gain of each stage is equal to the value of the voltage supply minus the threshold voltage of the N-channel MOSFET.

More sophisticated charge pumps have stages wherein the diode-connected MOSFET is replaced by a pass-transistor, and comprise circuits for boosting the gate voltage of the pass transistor. In this way, as long as the body effect on the threshold voltage of the pass-transistors is not very high, it is possbile to partially compensate the increase in the threshold voltage.

The main problem of these circuits resides in the fact that, due to the body effect, the threshold voltage of the N-channel MOSFETs becomes higher and higher moving from the stages proximate to the input terminal to the stages proximate to the output terminal of the charge pump. This causes a reduction in the voltage gain of the stages, and makes it necessary to increase the number of stages in order to generate a given output voltage.

A greater number of stages means a greater occupation of area in the chip, and a higher power consumption. Furthermore, it is not possible to generate output voltages higher than a given value, because when the threshold voltage (with body effect) of the N-channel MOSFETs becomes higher than the voltage supply, the addition of further stages is completely unuseful. Even the more sophisticated solution becomes less and less effective moving from the input terminal to the output terminal of the charge pump, and the final stages have a poor efficiency.

In view of the state of the art described, it is an object of the present invention to provide an improved positive charge pump which is not affected by the above-mentioned problem.

According to the present invention, such object is attained by means of a charge pump comprising a plurality of stages connected in series, an input terminal of the charge pump being connected to a voltage supply and an output terminal of the charge pump providing an output voltage higher than the voltage supply, each stage comprising unidirectional current flow MOS transistor means connected between a stage input terminal and a stage output terminal allowing current to flow only from said stage input terminal to said stage output terminal, and a first capacitor with one plate connected to said stage output terminal and another plate driven by a respective first digital signal periodically switching between ground and said voltage supply, characterized in that the unidirectional current flow MOS transistor means of the stages have independent bulk electrodes, and in that a bias voltage generator circuit is provided for biasing the bulk electrodes of said unidirectional current flow MOS transistor means at respective bulk potentials which become progressively higher going from the stages proximate to said input terminal to the stages proximate to said output terminal of the charge pump.

Thanks to the present invention, it is possible to completely eliminate the influence of the body effect on the threshold voltage of the unidirectional current flow MOS transistor means. The efficiency of the stages of the charge pump in terms of voltage gain remains substantially constant in going from the input terminal to the output terminal of the charge pump. It is thus possible to generate a given output voltage with a smaller number of stages, with a great reduction in chip area and power consumption.

The features of the present invention will be made apparent by the following detailed description of a particular embodiment thereof, illustrated as a non-limiting example in the annexed drawings, wherein:

Figure 1 is a circuit diagram of a positive charge pump according to one embodiment of the present invention;
Figure 2 is a timing diagram of drive signals for the charge pump of Figure 1;
Figure 3 is a circuit diagram of a bias circuit for the positive charge pump of Figure 1; and
Figure 4 is a cross-section showing two types of transistors for the circuits of Figures 1 and 3.

With reference to the drawings, in Figure 1 there is illustrated a positive charge pump according to one embodiment of the present invention. The charge pump comprises a plurality (four in this example) of stages S1-S4, connected in series between an input terminal I of the charge pump connected to a voltage supply VDD and an output terminal O of the charge pump. When the charge pump is integrated in an integrated circuit, such as for example a non-volatile memory device, VDD is the voltage supply of the device.

Each stage comprises a pass-transistor M1 formed by an N-channel MOSFET, connected between a stage input terminal SI and a stage output terminal SO; a capacitor C1 having one plate connected to the stage output terminal SO and another plate driven by a

respective phase signal B or D, depending on the particular stage; a precharge transistor M2 formed by an N-channel MOSFET with an electrode connected to the stage input terminal SI, another electrode connected to the gate electrode of M1 and a gate electrode connected to the stage output terminal SO; and a boosting capacitor C2 having one plate connected to the gate electrode of M1 and another plate driven by a respective phase signal A or C, depending on the particular stage. Signals A, B, C and D are generated by a timing signal generator 1.

The timing of signals A, B, C and D is depicted in Fig. 2. These signals are digital signals periodically switching between ground and the voltage supply; signals A and D are substantially in phase to each other, and the same holds true for signals B and C; signals A and D are respectively in phase opposition to signals B and C.

MOSFETs M1 and M2 in each stage have bulk electrodes which are independent from the bulk electrodes of MOSFETs M1 and M2 in the other stages.

The last stage S4 of the charge pump further comprises an N-channel MOSFET M13 with source connected to the stage input terminal SI, drain connected to the output terminal O of the charge pump, gate connected to the gate of M1 and bulk connected to the bulk of M1.

The charge pump further comprises a bias voltage generator 2 which generates three bias voltages B01, B2, B3. Bias voltage B01 is used to bias the bulk electrodes of MOSFETs M1 and M2 in the first and second stages S1 and S2; bias voltages B2 and B3 are used to bias the bulk electrodes of MOSFETs M1 and M2 in the third and fourth stages S3 and S4, respectively. For the generation of the bias voltages B01, B2 and B3, the bias voltage generator 2 is supplied with the output voltage O of the charge pump; the bias voltage generator 2 is also supplied with an enable signal EN.

It is to be observed that for an efficient biasing of the bulk electrodes of the MOSFETs M1 and M2 of the charge pump stages, two conflicting requirements must be taken into account: first, the bias voltage of the bulk electrode of MOSFETs M1 and M2 should be sufficiently high to limit the body effect; second, the voltage of the bulk electrode of the MOSFETs must always be lower or at most equal to the voltage of the source electrodes of the MOSFETs, to prevent forward biasing of the source/bulk junction.

Figure 3 is a circuit diagram of a preferred embodiment of the bias voltage generator 2 suitable to satisfy the above-mentioned requirements. The circuit comprises a voltage divider 3 formed by four diode-connected P-channel MOSFETs M3, M4, M5 and M6 connected in series between the output voltage O of the charge pump and ground. Bias voltage B3 is derived from a node N1 of the voltage divider between MOSFETs M3 and M4, with the interposition of a diode-connected P-channel MOSFET M7. Similarly, bias voltage B2 is derived from a node N2 of the voltage divider between M4 and M5, with the interposition of a diode-connected P-channel MOSFET M8, and bias voltage B01 is derived from a node N3 of the voltage divider between M5 and M6, with the interposition of a diode-connected P-channel MOSFET M9. Thus, bias voltages B3, B2 and B01 are respectively equal to:

$$V(B3)=V(O)*(R4+R5+R6)/RTOT-VTHP$$

$$V(B2)=V(O)*(R5+R6)/RTOT-VTHP$$

$$V(B01)=V(O)*R6/RTOT-VTHP$$

wherein R4, R5 and R6 are the output resistances of M4, M5 and M6, respectively, RTOT is the sum of the output resistances of M3, M4, M5 and M6, and VTHP is the threshold voltage of MOSFETs M7, M8 and M9. In other words, in order to generate the bias voltages for the bulk electrodes of MOSFETs M1 and M2 of the various stages, the output voltage V(O) of the charge pump is divided for the number of stages of the charge pump.

Connected to B3, B2 and B01 are respective filter capacitances C3, C4 and C5 with one plate connected to ground, which eliminate ripples on the voltages at nodes B3, B2 and B01, respectively. Also connected to nodes B3, B2 and B01 are respective N-channel MOSFETs M10, M11 and M12 with source connected to ground and gate driven by signal EN which, when the charge pump is disactivated (EN="1") forces V(B3), V(B2) and V(B01) to ground.

In operation, the circuit of Figure 3 ensures that the bias voltages V(B01), V(B2) and V(B3) are respectively equal to the lower among the voltages of the source and drain electrodes of MOSFETs M1 and M2 in stages S1, S2, S3 and S4 (as known, in a charge pump the source and drain electrodes of the MOSFETs are not univocally defined); thanks to this, the body effect on the threshold voltage of said MOSFETs is eliminated, and at the same time it is assured that the source/bulk junctions of the MOSFETs are not forward biased. MOSFETs M7, M8 and M9 introduce a safety margin sufficient to prevent that, due to possible spurious variations, the bias voltages V(B01), V(B2) and V(B3) directly bias the source/bulk junctions of the MOSFETs of the charge pump.

Thanks to the fact that the MOSFETs of the charge pump have independent bulk electrodes and thanks to the provision of the bias voltage generator 2 which biases the bulk electrodes of said MOSFETs, it is possible to minimize the number of stage of the charge pump required for generating a given output voltage; this means a reduction in the chip area and in the power consumption. Furthermore, it is possible to generate output voltages of any value, by simply adding stages to the charge pump: each stage will have a voltage gain which is not affected by the body effect. Biasing the bulk electrodes of the MOSFETs also increase the reliability

of the device, in fact when the MOSFETs are in the off condition the voltage applied to their gate oxide is lower.

Figure 4 shows in cross-section, side by side, a suitable structure of the N-channel MOSFETs M1 and M2 of the charge pump of Figure 1 and the structure of the P-channel MOSFETs M3-M9 of the bias voltage generator 2 of Figure 3. Each one of MOSFETs M1 and M2 is formed inside a respective P type well 4, formed in turn inside an N type well 5 provided in a P type substrate 6. Inside the P type well 4 two N+ regions 7 and 8 are formed, to form the source and drain electrodes of the MOSFET, and an insulated gate (gate electrode G of the MOSFET) is conventionally provided between regions 7 and 8; further, a P+ well contact region 9 is formed; a similar N+ well contact region 10 is formed inside the N type well 5. The P type well 4 and the P+ contact region 9 form the bulk electrode BUN of the MOSFET, and are short-circuited to the N+ contact region 10 to the N type well 5. In order to realize this structure, a so-called "triple well" manufacturing process is required; in fact, in order to have independent bulk electrodes which can be biased at different potentials, it is necessary that the bulk electrodes are electrically isolated from one another; this can be achieved by forming the N-channel MOSFETs inside separate P type wells 4 formed in turn inside separate N type wells 5; in a single or double well manufacturing process, the N-channel MOSFETs would be formed directly inside the P type substrate (which is normally kept grounded), and they would have a common bulk electrode.

Each one of the P-channel MOSFETs M3-M9 is instead formed inside a respective N type well 11; the bulk electrode BUP of such a MOSFET is formed by the N type well and by an N+ contact region 12 formed inside the N type well 11.

The previous description has been done referring by way of example to a particular charge pump circuit. However, it should be noted that the present invention can be applied in a straightforward way to different charge pump structures, for example those wherein each stage comprises only a diode-connected N-channel MOSFET and a capacitor.

Claims

1. Charge pump comprising a plurality of stages (S1-S4) connected in series, an input terminal (I) of the charge pump being connected to a voltage supply (VDD) and an output terminal (O) of the charge pump providing an output voltage higher than the voltage supply, each stage comprising unidirectional current flow MOS transistor means (M1) connected between a stage input terminal (SI) and a stage output terminal (SO) allowing current to flow only from said stage input terminal to said stage output terminal, and a first capacitor (C1) with one plate connected to said stage output terminal and another plate driven by a respective first digital signal (B,D) periodically switching between ground and said voltage supply, characterized in that the unidirectional current flow MOS transistor means (M1) of the stages have independent bulk electrodes (BUN), and in that a bias voltage generator circuit (2) is provided for biasing the bulk electrodes of said unidirectional current flow MOS transistor means at respective bulk potentials (B01,B2,B3) which become progressively higher going from the stages proximate to said input terminal to the stages proximate to said output terminal of the charge pump.

2. Charge pump according to claim 1, characterized in that said bulk potentials (B01,B2,B3) can be lower or higher than said voltage supply (VDD).

3. Charge pump according to claim 2, characterized in that each of said bulk potentials (B01,B2,B3) is at most equal to the minimum between a source voltage and a drain voltage of the respective unidirectional current flow MOS transistor means (M1).

4. Charge pump according to claim 3, characterized in that said bias voltage generator circuit (2) generates said bulk potentials (B01,B2,B3) starting from the output voltage of the charge pump.

5. Charge pump according to claim 4, characterized in that said voltage dividing means (3) comprise a voltage divider inserted between the output terminal of the charge pump and ground and having a number of intermediate nodes substantially equal to the number of stages of the charge pump.

6. Charge pump according to claim 5, characterized in that each of said bulk potentials (B01,B2,B3) is at most equal to the voltage of a respective intermediate node of the voltage partitioner (3).

7. Charge pump according to claim 6, characterized in that each of said bulk potentials (B01,B2,B3) is equal to the voltage of the respective intermediate node of the voltage partitioner (3), minus a prescribed voltage margin.

8. Charge pump according to claim 7, characterized in that each of said unidirectional current flow MOS transistor means comprises a diode-connected N-channel MOSFET.

9. Charge pump according to claim 7, characterized in that each of said unidirectional current flow MOS transistor means (M1) comprises an N-channel MOS field effect pass transistor, each stage further comprising gate voltage boosting means (M2,C2) for boosting a gate voltage of the pass transistor.

10. Charge pump according to claim 9, characterized in that said gate voltage boosting means (M2,C2) comprise an N-channel pre-charge MOSFET (M2) with first and second electrodes respectively connected to the stage input terminal (SI) and to the gate electrode of the pass MOSFET (M1) and a gate electrode connected to the stage output terminal (SO), and a second capacitor (C2) with one plate connected to the gate electrode of the pass MOSFET and another plate driven by a respective second digital signal (A,C) periodically switching between ground and the voltage supply and substantially in phase opposition with respect to the first digital signal (B,D).

11. Charge pump according to claim 1, characterized in that each of said unidirectional current flow MOS transistor means (M1) comprises a first well region (5) of a first conductivity type formed in a semiconductor substrate (6) of a second conductivity type, a second well region (4) of the second conductivity type formed inside the first well region, source and drain regions (7,8) of the first conductivity type formed inside the second well region (4) and an insulated gate disposed above the second well region between the source and drain regions, the second well region (4) forming the bulk electrode of the MOS transistor means being isolated from the substrate (6) by the first well region (5).

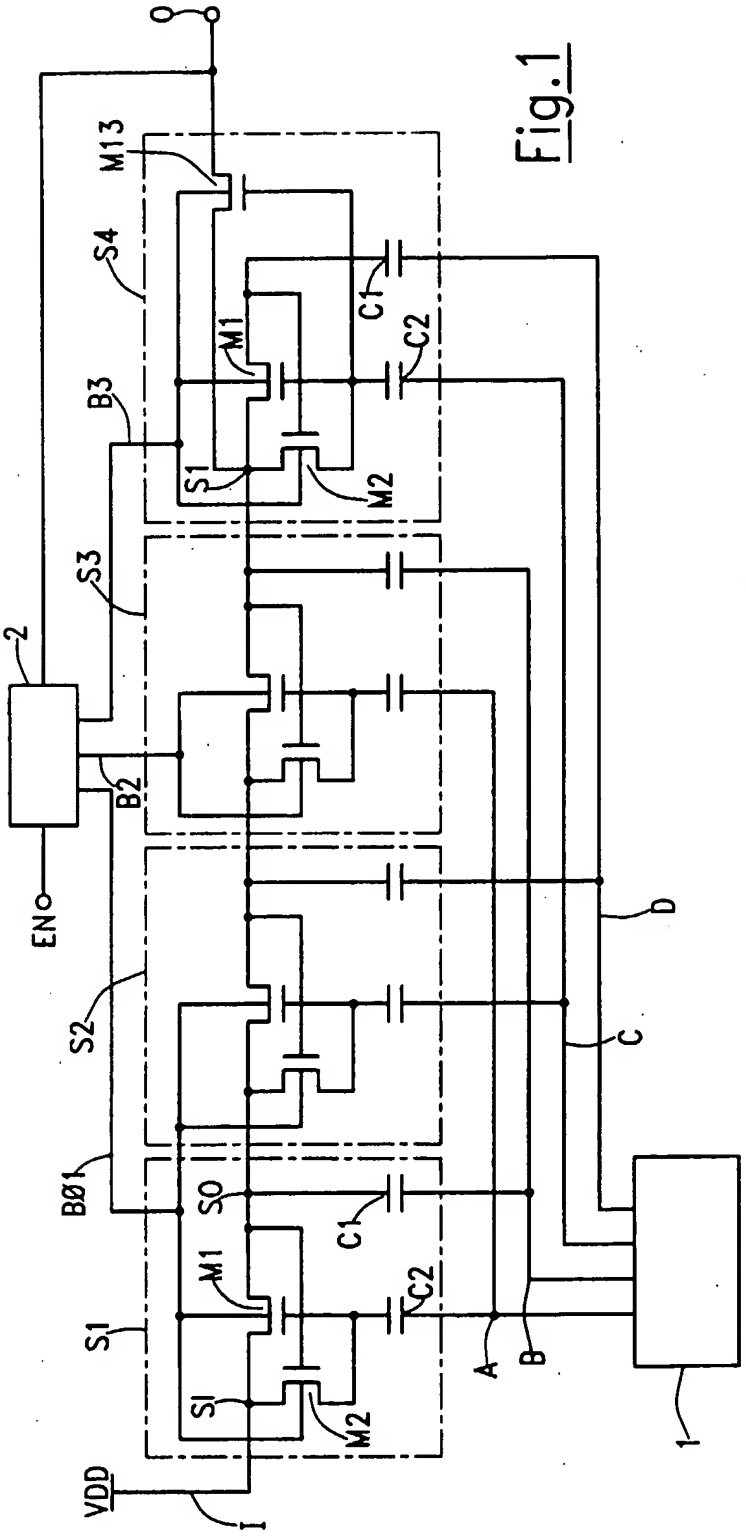
O
M13
S4
C1
C2
M1
B3
S1
M2
S3
2
B2
EN
S2
D
C
BØ1
SO
C1
M1
C2
S1
SI
M2
A
B
VDD
I
1

Fig.1

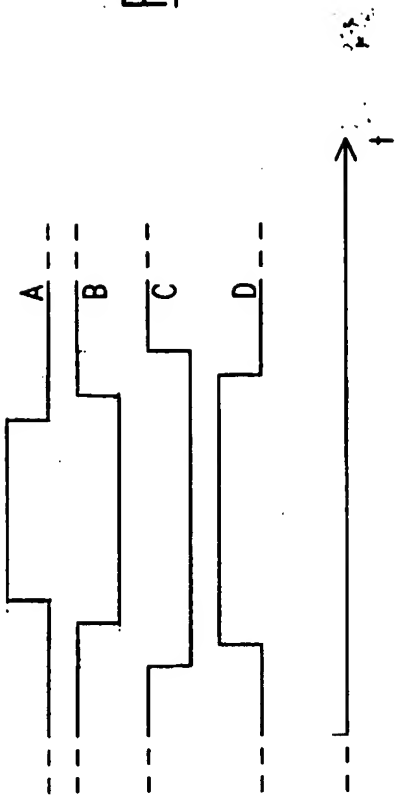
A
B
C
D
t

Fig.2

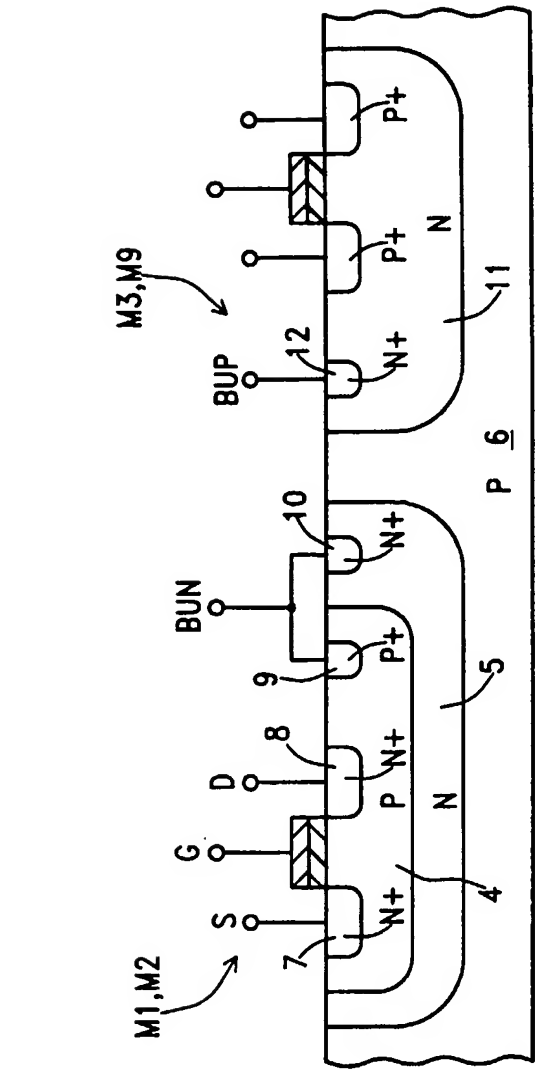
M3,M9
BUP
12
P+
N+
11
N
P 6
10
BUN
9
5
8
D
P
N+
G
4
S
7
M1,M2

Fig.4

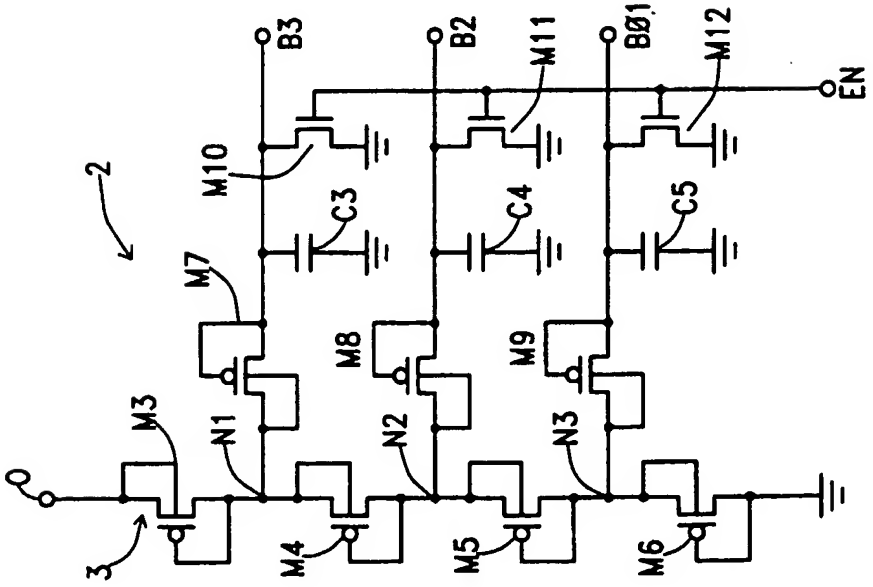
B3
B2
M11
BØ1
M12
EN
2
M10
C3
C4
C5
M7
M8
M9
M3
N1
N2
N3
3
M4
M5
M6

Fig.3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 83 0521

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 303 193 A (TOKYO SHIBAURA ELECTRIC CO) 15 February 1989 * column 4, line 24 - line 39; figure 4 * ---	1	H02M3/07
A	EP 0 445 083 A (SGS THOMSON MICROELECTRONICS) 4 September 1991 * page 1, line 23 - line 30; figure 1 * -----	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 February 1997	Van den Doel, J

CATEGORY OF CITED DOCUMENTS

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